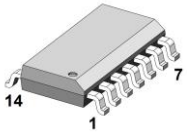
AS3944 – Array of matched 4 NPN transistors

Features

- low offset voltage . . . . . 200 µV
- high current gain 400
- matching guaranteed for all transistors

AS3944D



SOIC-14, 150 mil
1,27 pitch

General Description

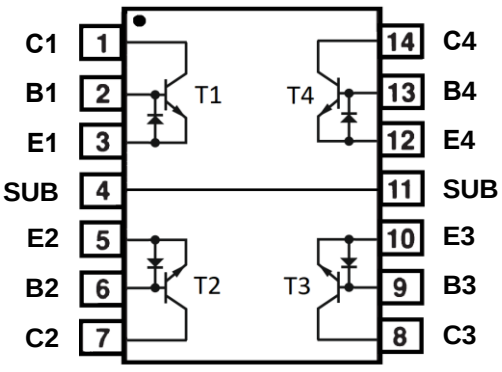
AS3944 is an array of 4 NPN transistor that offers excellent matching for precision amplifier and nonlinear applications. Performance characteristics include high gain over a wide range of collector current and Vcb, and excellent logarithmic conformance. AS3944 also features of low offset voltage µV and tight current gain matching. Each transistor is individually tested to data sheet specifications.

For matching parameters (offset voltage, input offset current, and gain match), each of the dual transistor combinations are verified to meet stated limits. The long-term stability of matching parameters is guaranteed by the protection diodes across the base-emitter junction of each transistor. These diodes prevent degradation of beta and matching characteristics due to reverse bias base-emitter current. Logarithmic conformance and accurate matching characteristics makes AS3944 an excellent choice for use in log and antilog circuits.

Pin Information

Pin No	Pin Name	Description
1	C1	Collector T1
2	B1	Base T1
3	E1	Emitter T1
4	SUB	Substrate
5	E2	Emitter T2
6	B2	Base T2
7	C2	Collector T2
8	C3	Collector T3
9	B3	Base T3
10	E3	Emitter T3
11	SUB	Substrate
12	E4	Emitter T4
13	B4	Base T4
14	C4	Collector T4

Pinout
Top view



Absolute Maximum Ratings

Collector - Base voltage (BV_{CBO})	40 V
Collector - Emitter (BV_{CEO})	40 V
Collector - Collector voltage (BV_{CC})	40 V
Emitter - Emitter voltage (BV_{EE})	40 V
Collector current	20 mA
Emitter current	20 mA

Electrical performance characteristics

(Tamb = 25 ºC)

Parameter	Symbol	Conditions	AS3944			Unit
			Min	Typ	Max	
Current Gain	h_{FE}	U_{CB} = 0 V to 30 V (Note 1) 10 µA < I_C < 1 mA	400	800	-	-
Current Gain Match, $\Delta h_{FE1,2,3,4} = 100[\Delta I_B]\,[h_{FE(MIN)}] / I_C$	Δh_{FE}	U_{CB} = 0 V to 30 V I_C = 100 µA	-	0,5	2	%
Current Gain Match, $\Delta h_{FE1,2,3,4} = 100[\Delta I_B]\,[h_{FE(MIN)}] / I_C$	Δh_{FE}	U_{CB} = 0 V to 30 V I_C = 10 µA to I_C = 1 mA		0,5		%
Emitter - Base Offset Voltage	V_{OS}	(Note 2) U_{CB} = 0 V to 30 V I_C = 10 µA to I_C = 1 mA	-	50	200	µV
Change in Emitter - Base Offset Voltage vs. Collector - Base Voltage	CMRR	(Note 2) I_C = 10 µA to I_C=1 mA U_{CB} = 0 V to 30 V	-	50	200	µV
Change in Emitter - Base Offset Voltage vs. Collector Current	$\Delta V_{OS} / \Delta I_C$	(Note 3) U_{CB} = 0 V I_C = 10 µA to 1 mA	-	5	50	µV
Breakdown Voltage	BV_{CEO}	I_C = 10 µA	40	-	-	V
Collector - Base Leakage	I_{CBO}	U_{CB} = 40 V	-	5	-	nA
Collector - Collector Leakage	I_{CCO}	U_{CC} = 30 V	-	0,2	5	nA
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	I_C = 1 mA, I_B = 100 µA	-	0,03	0,06	V

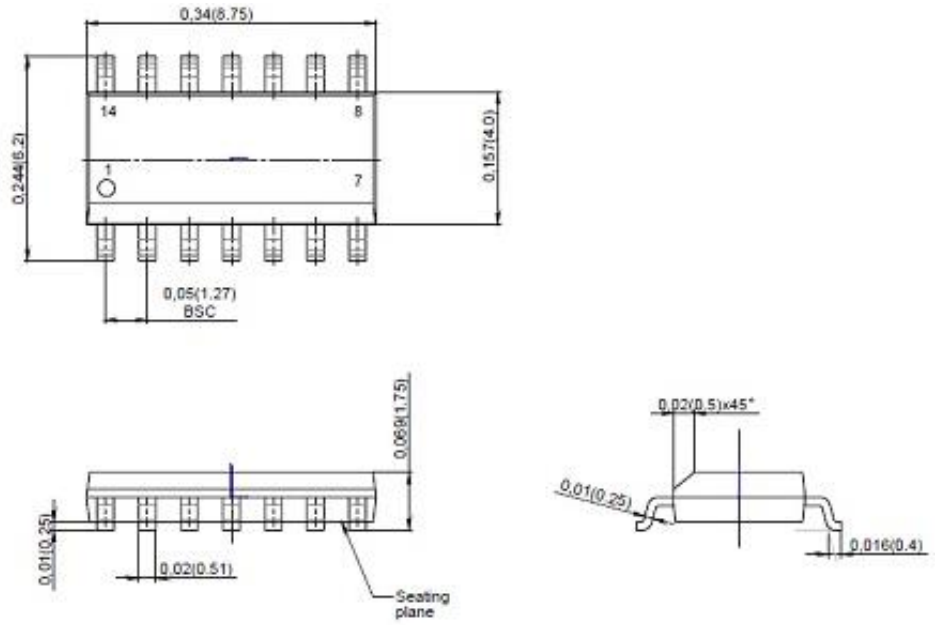
Note 1: Collector-base voltage is swept from 0 to U_{MAX} = 30 V at a collector current of 10 µA, 100 µA and 1 mA.

Note 2: Measured at I_C = 100 µA, for pairs T1-T2, T1-T3, T3-T4 and guaranteed by design over the specified range of I_C.

Note 3: Measured from I_C = 10 µA to I_C = 100 µA, for pairs T1-T2, T3-T4 and guaranteed by design over the specified range of I_C.

Device type	Package
AS3944D	SOIC-14 (150 Mil)

Package Dimensions in millimeters
SOIC-14 (150 mil)



Revision history

Date	Revision	Changes
04-May-2021	**1**	Preliminary version 1
27-Sep-2021	**2**	Preliminary version 2