AS3207DA, AS3207DB – 1024 stage BBD

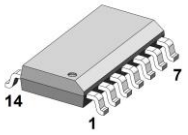
Features

- Variable delay of audio-signals: 1.3 ms ~ 50.2 ms
- Clock frequency . . . . . 10 kHz – 200 kHz
- Low distortion: THD ≤ 2% (Vin = 0.7 V rms)
- Maximum input voltage . . . . . 3 V_{p-p}
- Operation temperature -20 ~ +60° C
- 14-lead SOIC package

Applications

- Sound effects in electronic musical instruments
- Variable or fixed delay of analog signals

AS3207D



SOIC-14 150mil, 1.27 mm

General Description

AS3207D is a 1024-stage Bucket-Brigade Device (BBD). AS3207D benefits from its output split into two channels, so that output is provided over each full clock period.

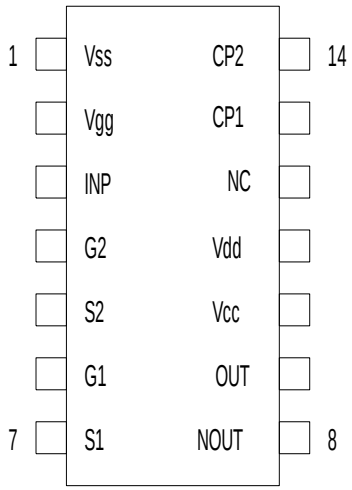
Negative offset on substrate referenced to low level of CP1 and CP2, separate supply of output source followers, additional matched transistors, with external circuitry, gives opportunity to increase dynamic range and improve THD.

N - channel silicon gate process.

Pin Information

Pin No	Pin Name	Description
1	Vss	Substrate
2	Vgg	BBD gate supply
3	INP	BBD Input
4	G2	Gate transistor 2
5	S2	Source transistor 2
6	G1	Gate transistor 1
7	S1	Source transistor 1
8	NOUT	Inverse Output BBD
9	OUT	Output BBD
10	Vcc	Output stage supply
11	Vdd	BBD supply
12	NC	Not connected
13	CP1	Clock pulse 1
14	CP2	Clock pulse 2

Terminal Assignments



Absolute Maximum Ratings
Unless otherwise specified, T_A = 25ºC

Parameters	Symbol	Value	Units
BBD voltage supply	V_{DD}	+9	V
Output stage voltage supply	V_{CC}	+9	V
Maximum voltage CP1, CP2	$V_{CP1\ ,\ CP2}$	≤ V_{DD}	V
Minimum voltage CP1, CP2	$V_{CP1\ ,\ CP2}$	≥ V_{SS}	V
Input voltage	V_{INP}	V_{SS} < V_{INP} < V_{DD}	V
Storage Temperature Range	Tstg	-55~+85	ºC
Operating Temperature Range	Topr	-20~+60	ºC
Junction Temperature Range	Tj	-55~+150	ºC

Operation Condition
Unless otherwise specified, T_A = 25ºC

Parameters	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	+4	+5	+9	V
Output Stage Supply Voltage	V_{CC}	+4	+7	+9	V
Gate Supply Voltage	V_{GG}	13/15 V_{DD}	14/15 V_{DD}	V_{DD}	V
Substrate Voltage	V_{SS}	-3	-2	0	V
Clock Voltage "H"	Vcph	V_{DD} - 0.5 V	V_{DD}	V_{DD}	V
Clock Voltage "L"	Vcpl	-0.3	0	0.5	V
Clock Pulse Rise Time	tcpr	50	200	500	ns
Clock Pulse Fall Time	tcpf	50	200	500	ns
Clock Frequecy	Fcp	10	40	200	kHz

Electrical Characteristics
(V_{DD} = +5V, V_{CC} = +7V, V_{GG} = 14/15·V_{DD} , V_{SS} = -2V, $V_{MAX\ /\ MIN\ CP1,CP2}$ = +5V / 0V; R_L = 100 kΩ; using typical application circuit Fig.2 , typical specifications apply at T_A = +25°C.)

Parameters	Symbol	Conditions	Min	Typ	Max	Units
Supply current	Idd	Fcp = 100 kHz, V_{DD}=5 V			100	uA
Supply current	Icc	Fcp = 100 kHz, V_{CC}=7 V	100	120	150	uA
Bias voltage*	Vbb	Fcp = 40 kHz	1.7	2.4	3	V
Maximum input signal swing (A)	Vin p-p	Fcp = 40 kHz; THD ≤ 2%	2.0			V
Maximum input signal swing (B)			1.7			
Distortion (A)	THD	Vin = 0.7 Vrms; Fin=1 kHz		1.5	2	%
Distortion (B)		Vin = 0.6 Vrms; Fin=1 kHz		0.5	2	
Gain	Gi	Fcp = 40 kHz	0.9	1.3	1.5	
Insertion Loss	Li	Fcp = 100 kHz; Fin=1 kHz	-4	3	4	dB
Sampling frequency	Fcp	3 dB point	10	40	200	kHz
Clock line capacitance	Ccp			140		pF
Input capacitance	Cin			2.6		pF
Signal freq. bandwidth (3dB point)	BW	Fcp = 200 kHz	25	30	35	kHz
Output resistance OUT, NOUT	Ro			500		Ohm
Output Noise Voltage	Vno	Fcp = 200 kHz		0.4		mVrms

*Bias voltage of input signal must be set on the middle of linear region (See Fig.3)

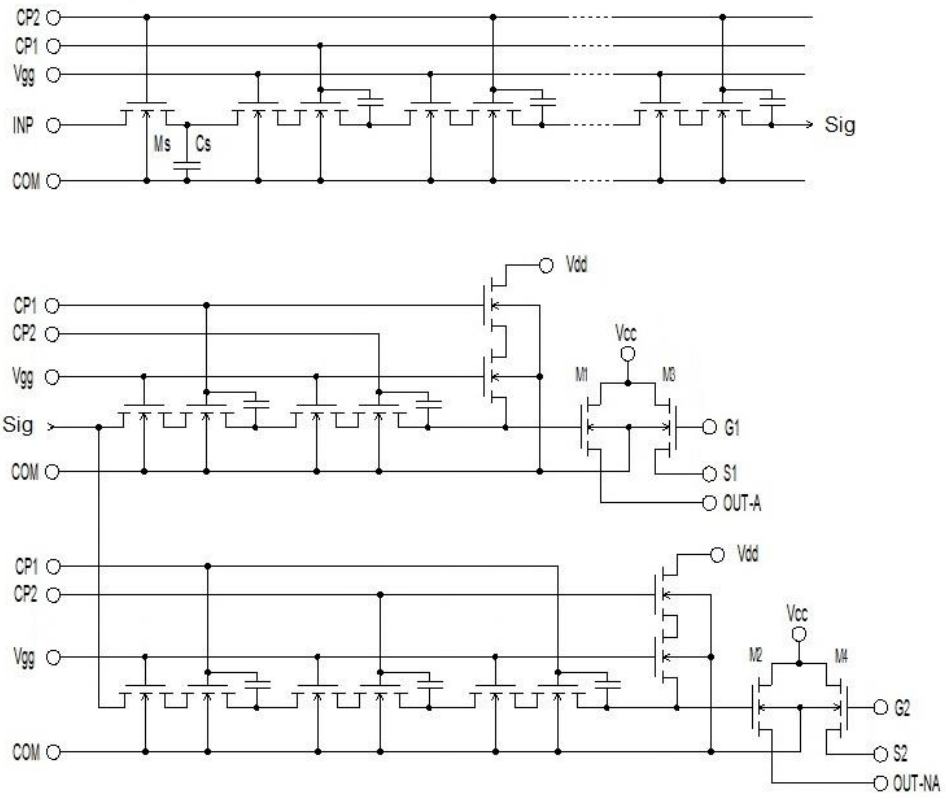


Figure 1. Equivalent Circuit-Diagram.

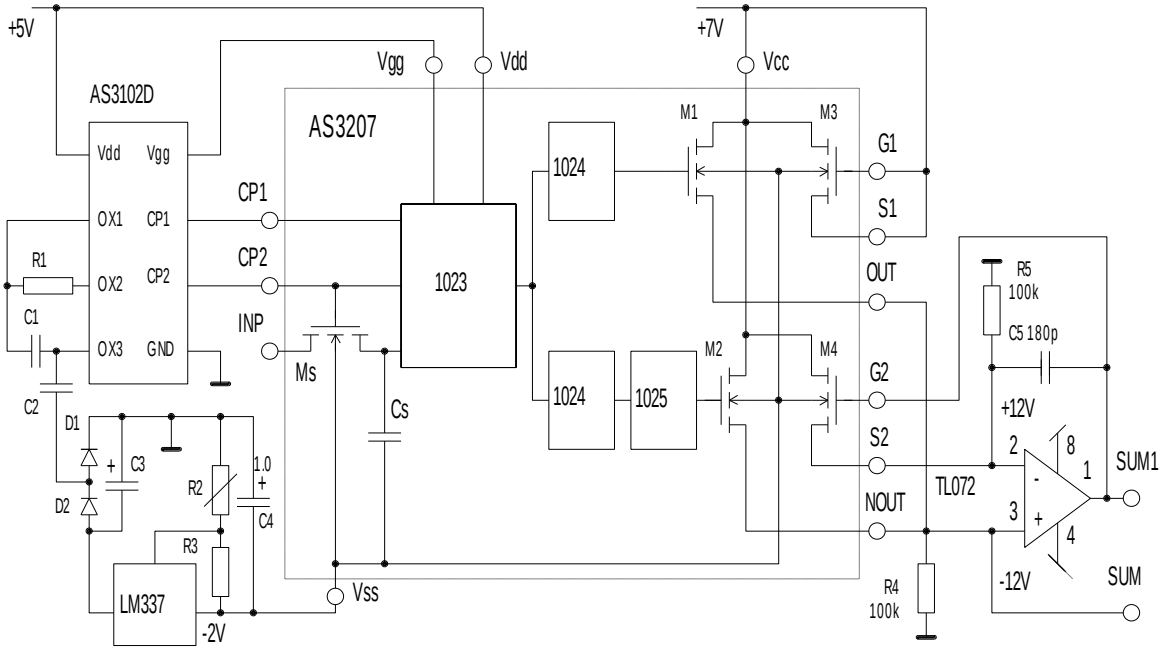


Figure 2. Typical Application Circuit.

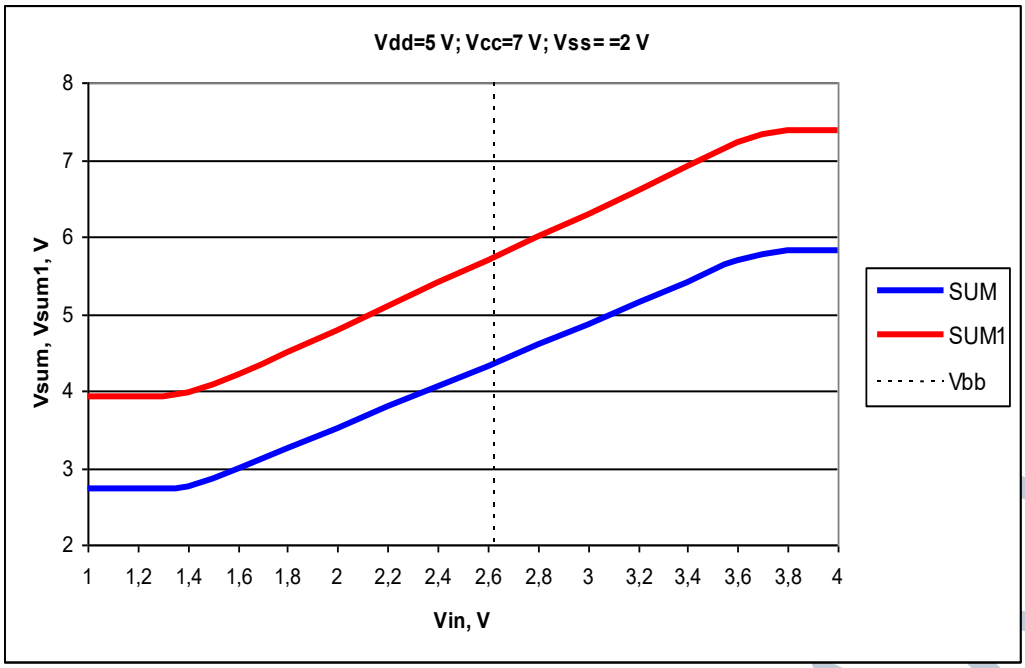


Figure 3. Transfer Characteristic.

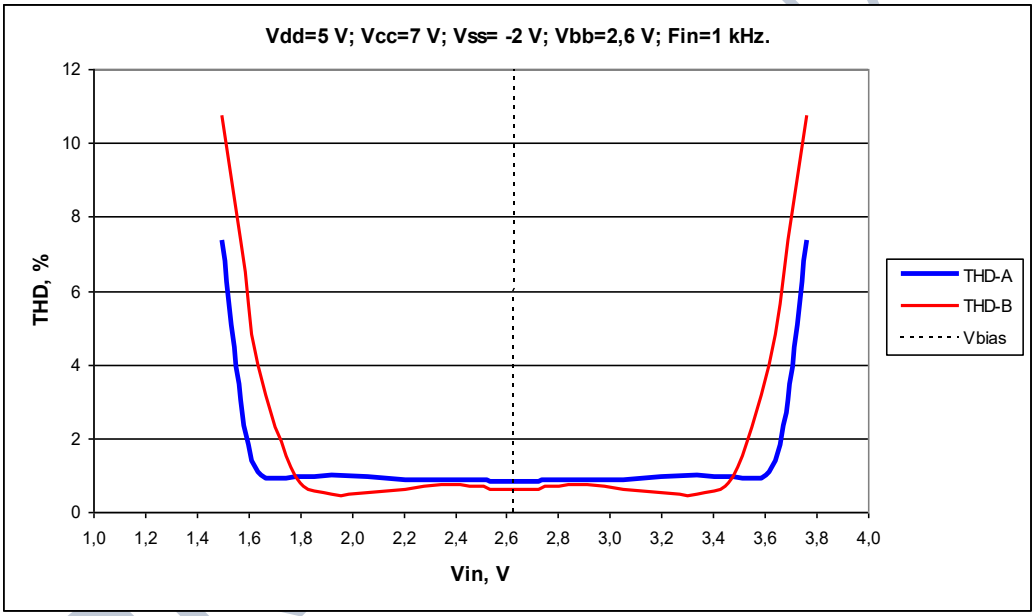


Figure 4. Distortion vs. Input Level.

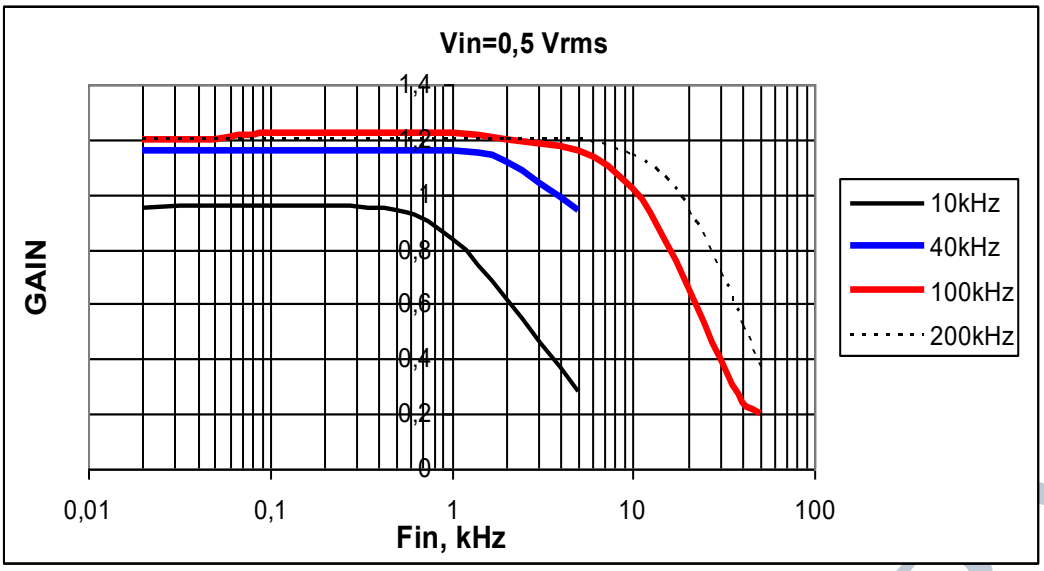


Figure 5. Gain v.s. Input Frequency.

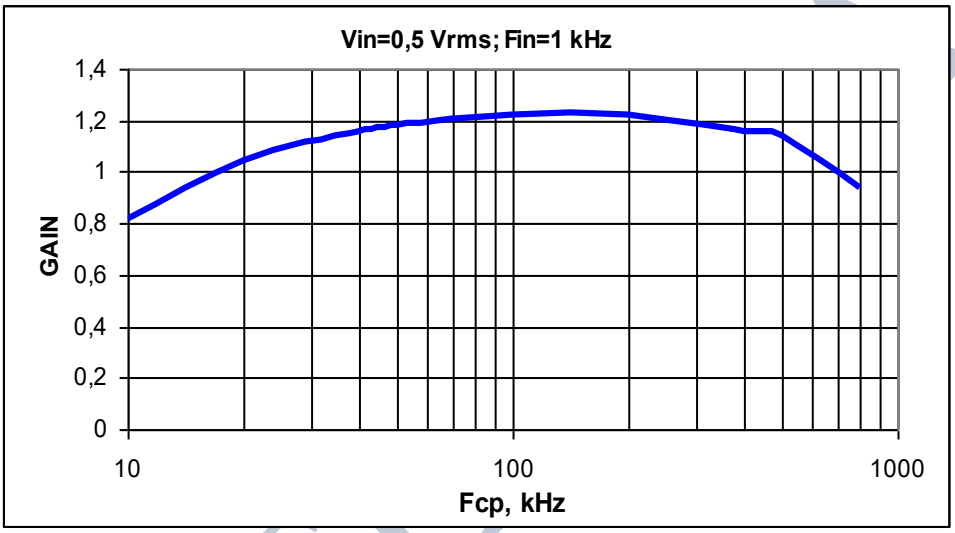


Figure 6. Gain v.s. Clock Frequency

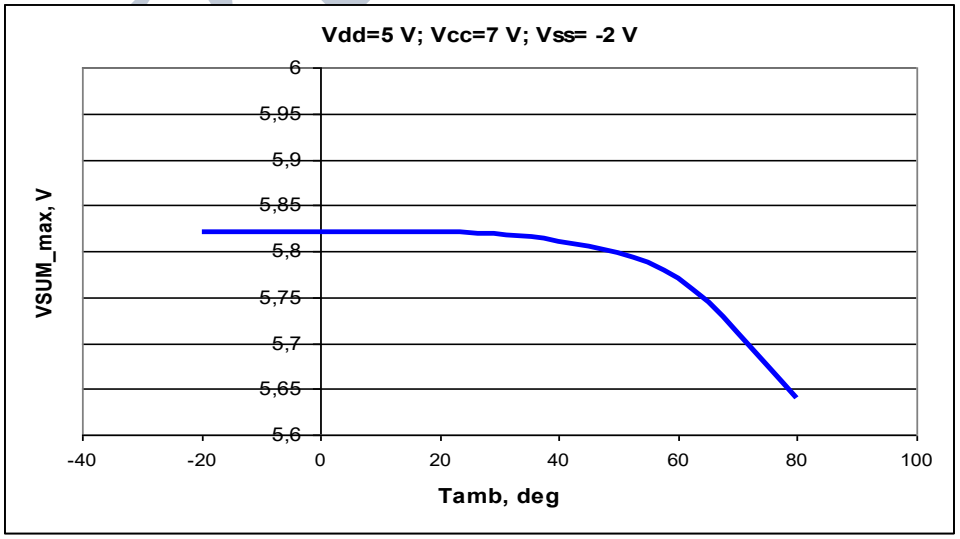


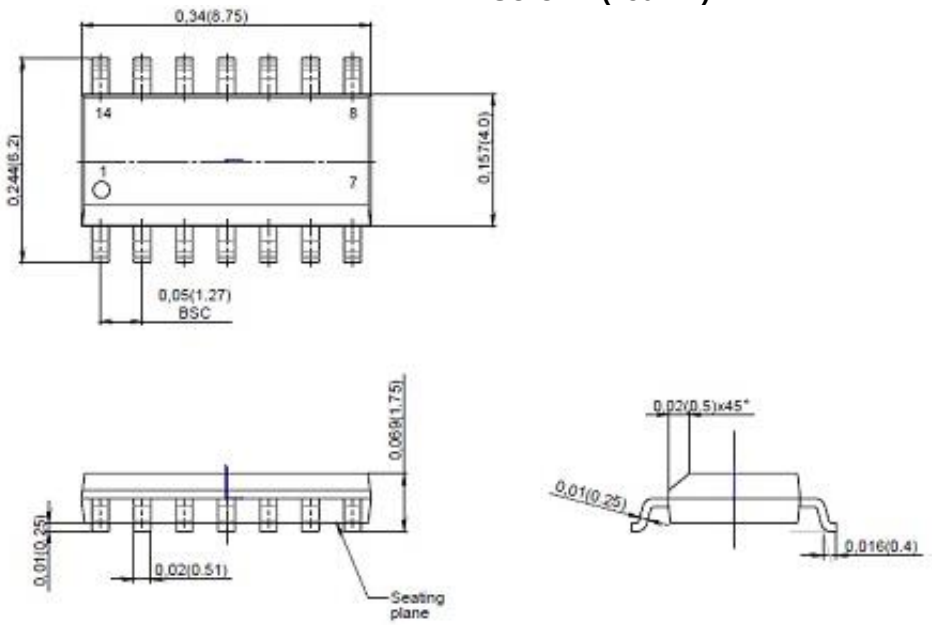
Figure 7. Maximal Output Voltage v.s. Temperature.

Device type	Package
AS3207D	SOIC-14 (150mil)

OUTLINE DIMENSIONS

Dimensions show in inches and (millimeters)

SOIC-14 (150 mil)



Revision history

Date	Revision	Changes
20-Jan-2022	1	Initial version